Dr. AMIT KUMAR PANDEY
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OBJECTIVE: To be creative, competent and successful through hard work and determination, to be the part of the organization.

ACADEMIC QUALIFICATIONS:

- Bachelor of Engineering in Electronics from Swami Ramanand Teerth Marathwada University, Nanded, Maharashtra in 2001 with 72% (I^{st} Div).
- Master of Technology in Control and Instrumentation from NIT Allahabad, in 2004 with 78% (I^{st} Div with Distinction).
- Doctor of Philosophy in Electronics and Communication Engineering from NIT Allahabad in 2014 with CPI=9.5.

SPECIALIZATION: VLSI Design

AREA OF RESEARCH: VLSI circuit, Low power circuits.

PROJECTS:

- **Ph.D Dissertation: Performance evaluation of Domino CMOS circuits for low voltage VLSI design**
  Domino Circuits are widely used in high-speed applications for the implementation of high fan-in circuits. The noise sensitivity of domino circuits is due to their low switching threshold voltage, which is equal to the threshold voltage of NMOS devices in the evaluation network. The substantial increase in deep-submicron noise with technology scaling impacts the usefulness of domino circuits with technology scaling, the supply voltage is scaled down to decrease the power consumption. The main source of noise in deep-submicron circuits is mainly due to the high leakage current, crosstalk noise, supply noise, and charge-sharing. As the technology scales down, the leakage of the evaluation transistors exponentially increases due to lower threshold voltage. To solve the problem of high subthreshold and gate oxide leakage current, many circuit level techniques have been proposed including body bias control, input vector control, transistor stack effect, dual V_t CMOS, sleep switch. Dual-V_t domino technique is realized by using low-V_t transistor in the evaluation path and high-V_t transistor in the precharge path of the circuits. To demonstrate this problem on the tools Hspice, layout is drawn on Cadence. Finally, circuits are made on the chip, so measurement results are taken and make comparison to the simulation result

- **M.Tech Dissertation: Power factor improvement of boost converter**
  Now a day's DC-DC converter (Chopper) is using for the interfacing the DC loads with the AC main line supply. The main function of the Chopper is to utilize the maximum active power from the main supply and transfer to the

load. With the help of DC-DC converters we can improve the power factor for the Universal Input Application. In the proposed work using a new two dependently switch topology of Boost Converter we can improve the Power Factor, reduce the Total Harmonic distortion, voltage and current stress on the switch and also increase the efficiency of the converter. For this proposed converter average current control scheme offered which sense the input current and compared to the reference sinusoidal current with the help of current loop amplifier. The main function of the CEA is to reduce the error between the input current and the reference current and its output handle the switching period for the two switches which is using in the converter.

ACADEMICS EXPERIENCE:

- Worked as Lecturer**,** Department of Electronics and Communication Engineering, NIT Allahabad, Uttar Pradesh. **Jan, 2003 – Jan,2004**
- Worked as Assistant Professor**,** Department of Electronics and Communication Engineering, Raj Kumar Goel Institute of Technology, Ghaziabad, Uttar Pradesh. **Feb, 2005 – Dec,2009**
- Worked as Associate Professor in Department of Electronics and Communication, Raj Kumar Goel Institute of Technology, Ghaziabad, Uttar Pradesh. **Jan,2014 – Dec, 2017**
- Working as Assistant Professor in Department of Applied Science and Humanities**,** Rajkiya Engineering College, Ambedkar nagar, Akbarpur, Uttar Pradesh. **Dec,2017-Till date**

Subjects Taught:

- Basic Electronics
- Electromagnetic field theory
- Analog Integrated Circuits
- Digital electronics
- Control systems
- VLSI Design
- Communication Engineering

RESEARCH PAPERS:

Journal

1. A. Gupta, M. Rai, A. K. Pandey, S. Rai, D. Pandey, "A Novel Approach to Investigate Analog and Digital Circuit Applications of Silicon Junctionless-Double-Gate (JL-DG) MOSFETs", Silicon Springer.
2. A. K. Pandey, T. K. Gupta, A. Gupta, and D. Pandey, "Keeper Effect on Nano Scale Silicon Domino Logic Transistors", Silicon Springer.
3. V. Gupta, N. Kumar, H. Awasthi, S. Rai, A. K. Pandey, A. Gupta, "Temperature- dependent analytical modelling of graded-channel gate-all around (GC-GAA) junctionless field-effect transistors (JLFETSs)", Journal of Electronics Materials, Springer, vol. 50, pp. 3686-3691, 2021**.**
4. V. Gupta, H. Awasthi, N. Kumar, A. K. Pandey, A. Gupta, "A novel approach to model threshold voltage and subthreshold current of graded-doped junctionless-gate-all-around (GD-JL-JAA) MOSFETS", Silicon Springer, vol. 29.
5. **S. Upadhyay, A. K. Pandey, and S. K. Pandey, "**Performance Evaluation of Low Power Adiabatic Techniques", TEXT Engineering and Management, vol.82, pp. 4132-4137.

6. S. Garg, T. K. Gupta, and A. K. Pandey, “A 1-bit full adder using CNFET based dual chirality high speed domino logic”, International Journal Circuit theory and Applications, pp.1-19, 2019.
7. S. Garg, T. K. Gupta, and A. K. Pandey, “4:1 Multiplexer Using Dual Chirality CNTFET Based Domino Logic In Nano-Scale Technology”, International Journal of Electronics, vol. 107, no. 4, pp. 513-541, 2020.
8. A. K. Pandey, S. Upadhyay, T. K. Gupta, and P. K. Verma, “Low power, high speed and noise immune wide-OR footless domino circuit using keeper controlled method”, Analog Integrated Circuits and Signal Processing, pp. 1-13.
9. A. K. Pandey, T. K. Gupta, and P. Verma, "Sleep signal controlled footless domino circuit for low leakage current", Circuit World, Emerald Publisher, vol.44, no. 2, pp. 87-98, 2018.
10. A. K. Pandey, P. Verma, R. Verma, and T. K. Gupta, " Analysis of noise immunity for wide OR footless domino circuits using keeper controlling network", Circuits Systems and Signal Processing, Springer, 2018
11. T. K. Gupta, A. K. Pandey, and O. P. Meena, “Analysis and Design of Lector Based Dual-Vt Domino Logic with Reduced Leakage Current”, Circuit World, Emerald Publisher, vol.43, pp.97-104, 2017
12. A. K. Pandey, V. Mishra, R. A. Mishra, R. K. Nagaria, and V. K. Rao, “Conditional precharge dynamic buffer circuit”, International Journal of Computer Applications, vol. 60, no. 6, pp.45-52, December 2012.
13. A. K. Pandey, R. A. Mishra, and R. K. Nagaria, “Low power dynamic buffer circuits”, International Journal of VLSI Design & Communication Systems (VLSICS), vol. 3, no. 5, October 2012.
14. A. K. Pandey, R. A. Mishra, and R. K. Nagaria, “Leakage power analysis of domino XOR gate”, ISRN Electronics, Hindawi, volume 2013, Article Id 271316, pp.1-7, January 2013.
15. A. K. Pandey, J. Tiwari, R. A. Mishra, R. K. Nagaria, and M. Tiwari, “Design of new low leakage power domino XOR circuit”, International Journal of Computer Applications, vol. 65, no.1, pp.28-32, March 2013.
16. A. K. Pandey, R. A. Mishra, and R. K. Nagaria,” Static switching dynamic buffer circuit”, Journal of Engineering, Hindawi, volume 2013, Article Id 646214, pp.1-11, March 2013.
17. A. K. Pandey, R. A. Mishra. and R. K. Nagaria, “Performance analysis of novel domino XNOR gate in sub 45n CMOS technology”, WSEAS Transactions on Circuits and Systems, vol.12, no.2, pp48-57, February 2013.
18. A. K. Pandey, V. Mishra, R. A. Mishra, R. K. Nagaria, and V. K. Rao,” Design of a trigger pulse operated low power domino circuit”, The Mediterranean Journal of Electronics and Communication, vol.9, no.1, pp.485-493, January 2013.
19. A. K. Pandey, R. A. Mishra, and R. K. Nagaria, “New noise tolerant domino logic circuits”, World applied sciences Journal, vol.27, no.2, pp.257-268-57, December 2013.
20. A. K. Pandey, R. A. Mishra, and R. K. Nagaria, “Leakage power analysis of dynamic footed circuits in 45nm CMOS Technologies”, African Journal of Basic and applied sciences, vol.5, no.6, pp.268-275, 2013.

Conference

1. A. K. Pandey, R. A. Mishra, and R. K. Nagaria, “Low leakage power in sub-45nm with multiple threshold voltages and multiple gate-oxide thickness footed domino circuits”, IEEE Conference, Nirma University, Ahmedabad, pp.1-6,08-10 December 2011.
2. P. Rani, A. K. Pandey, R. A. Mishra, and R. K. Nagaria, “A survey on different keeper design topologies for high speed wide AND-OR domino circuits”, IEEE Student Conference, pp.1-4, 16-18 March, 2012.
3. A. K. Pandey, S. Kaur, R. A. Mishra, and R. K. Nagaria, “Leakage power reduction for domino circuits in 45 nm CMOS technologies”, IEEE Conference (ICPCES), MNNIT Allahabad,17-19 December 2012.

4. S. Kumar, S. Singhal, A. K. Pandey, and R. K. Nagaria, “Design and simulation of low power dynamic logic circuit using footed diode domino logic”, IEEE Student Conference, MNNIT Allahabad, pp.1-4, 2013.
5. Y. K. Mohan, A. K. Pandey, R. K. Singh, and R. K. Nagaria, “New domino logic designs for static outputs in evaluation phase for high frequency inputs”, IEEE Student Conference, MNNIT Allahabad, pp.1-6, 2013.

PERSONAL INFORMATION:

Father's name:	Raj Kishore Pandey
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